Claims

What is claimed is:

1. A metal-oxide-semiconductor (MOS) device, comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

at least one contact, the at least one contact comprising:

a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and

at least one insulating layer formed directly on the silicide layer.

2. The device of claim 1, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

3. The device of claim 1, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

4. The device of claim 1, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

5. The device of claim 1, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.

6. The device of claim 1, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

7. The device of claim 1, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

8. The device of claim 1, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

9. The device of claim 8, wherein the MOS device comprises a lateral DMOS (LDMOS) device.

10. A method for forming a metal-oxide-semiconductor (MOS) device, comprising the steps of:

forming a gate proximate an upper surface of a semiconductor layer, the semiconductor layer being of a first conductivity type;

forming first and second source/drain regions of a second conductivity type in the semiconductor layer proximate the gate, the gate being between the first and second source/drain regions;

forming a silicide layer on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and

forming at least one insulating layer directly on the silicide layer.

11. The method of claim 10, wherein the step of forming the first source/drain region comprises:

forming an n-type region and a p-type region in the semiconductor layer, wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

12. The method of claim 10, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

13. The method of claim 10, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

14. The method of claim 10, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.

15. The method of claim 10, further comprising the step of forming a shielding structure proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

16. The method of claim 10, wherein the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

17. The method of claim 10, wherein the MOS device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

18. The method of claim 17, wherein the MOS device comprises a lateral DMOS (LDMOS) device.

19. An integrated circuit (IC) device comprising a plurality of metal-oxide semiconductor (MOS) devices, at least one of the MOS devices comprising:

a semiconductor layer of a first conductivity type;

a first source/drain region of a second conductivity type formed in the semiconductor layer;

a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region;

a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions; and

at least one contact, the at least one contact comprising:

a silicide layer formed on and in electrical connection with at least a portion of the first source/drain region, the silicide layer extending laterally away from the gate; and

at least one insulating layer formed directly on the silicide layer.

20. The IC device of claim 19, wherein the first source/drain region comprises an n-type region and a p-type region, and wherein the silicide layer is formed substantially proximate the n-type and p-type regions such that the silicide layer forms a substantially low-resistance electrical path in parallel with an electrical path formed between the n-type and p-type regions.

21. The IC device of claim 19, wherein substantially all current associated with the first source/drain region passes through the silicide layer in a direction from the first source/drain region to a region having a conductivity type opposite the first source/drain region that is proximate the upper surface of the semiconductor layer.

22. The IC device of claim 19, wherein the at least one insulating layer comprises at least one conductive layer, the at least one conductive layer being electrically isolated from the silicide layer.

23. The IC device of claim 19, further comprising a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate.

24. The IC device of claim 19, wherein the device comprises a diffused MOS (DMOS) device, the first source/drain region comprises a source region and the second source/drain region comprises a drain region.

25. The IC device of claim 19, wherein the silicide layer forms a substantially low-resistance electrical path for conducting current between two or more regions in the semiconductor layer that are electrically isolated from the device.